

APPENDIX A

ELECTRONIC CIRCUIT DETAILS

A.1 Measurement of Conductance–Voltage Characteristics

A.1.1 Circuit Design

Circuits used to measure current–voltage and conductance–voltage characteristics are illustrated in figures 5.1 and 5.2. This section discusses their design and construction.

A.1.1.1 Sample-Biasing Electronics

OPA111 operational amplifiers were used to voltage bias the sample (OP1 and OP2 in chapter 5). These were selected because of their low noise, low input bias currents (1 pA) and low offset and drift characteristics. To prevent degradation of the drift performance offset adjustment was not used; however, the resulting 0.25 mV offset at the sample was subtracted by software when calibrating the raw data.

A very low phase-shift OPA633 buffer amplifier was placed in the OPA111's feedback loop (figure A.1). This enabled the circuit to produce large currents of 100 mA at the maximum sample bias of 1 V, removed load-dependent voltage drift and prevented feedback instabilities when driving capacitive loads (Horowitz and Hill 1980, p.277). The OPA633 was mounted in a DIP socket for easy replacement if damaged by excessive currents, whilst output-protection circuitry was used to minimise the possibility of damage occurring. These precautions prevented any damage to the OPA111 op-amps and allowed these to be soldered directly to the PCB as recommended by the manufacturer (Burr-Brown).

The d.c. voltage input to the sample-biasing electronics was provided by a DAC in the CIL6580 unit, controlled by computer via an RS-232 interface. To use the full 16-bit resolution of the DAC, the output voltage ramp was always defined to be between ± 10 V and was attenuated to the required full-scale sample bias by an adjustable potential divider.

A simple low-pass RC filter was added to the potential divider to attenuate high-frequency noise (>10 kHz) generated by the DAC (figure A.2). The resulting attenuation was given by

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{(1 + R_1 / R_{\text{atten}}) + j\omega C(R_1 R_2 / R_{\text{atten}} + R_1 + R_2)}$$

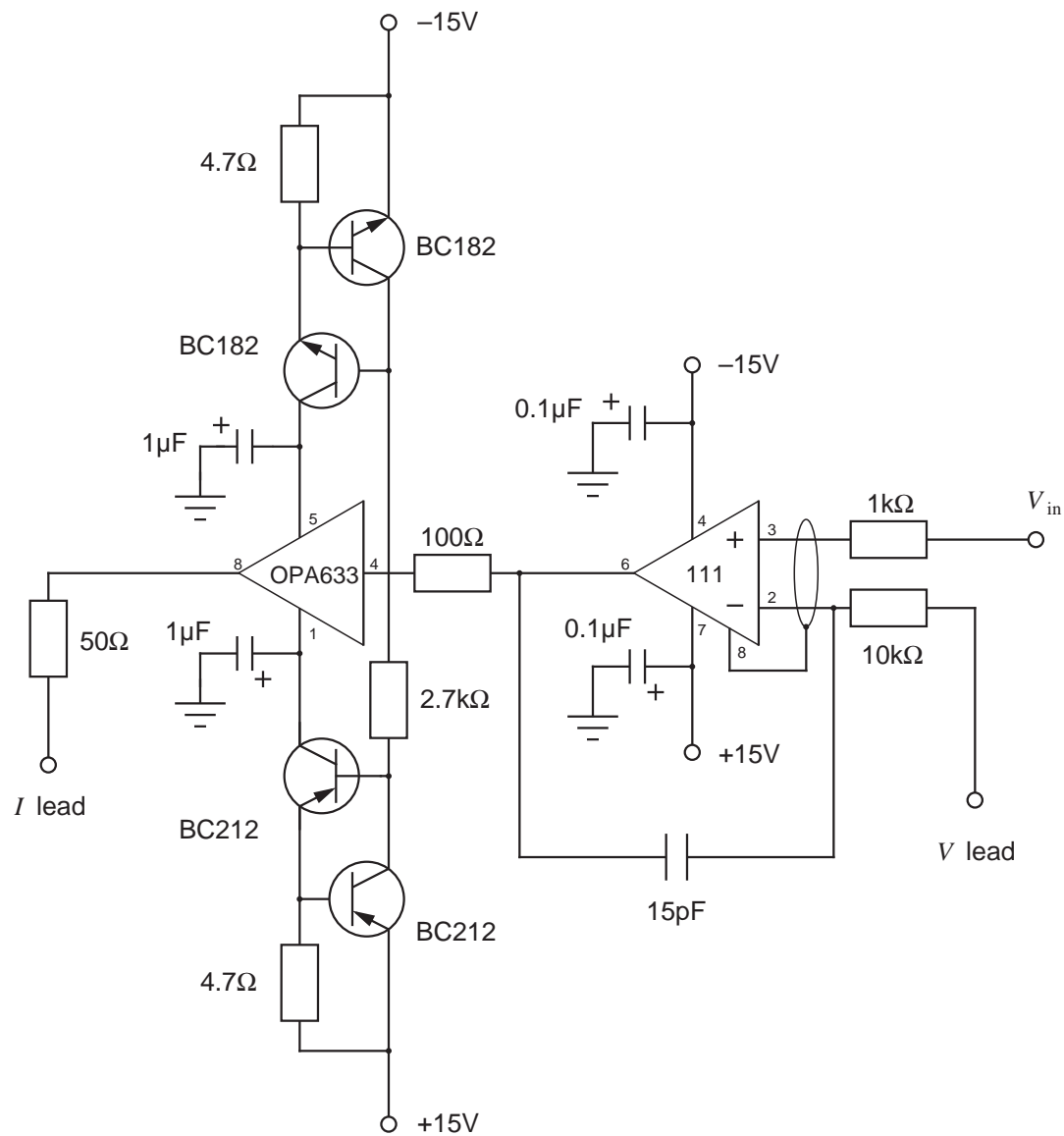


Fig. A.1. Construction of the sample-biasing op-amps, OP1 and OP2. This shows the high-speed buffer amplifier and its output protection circuitry.

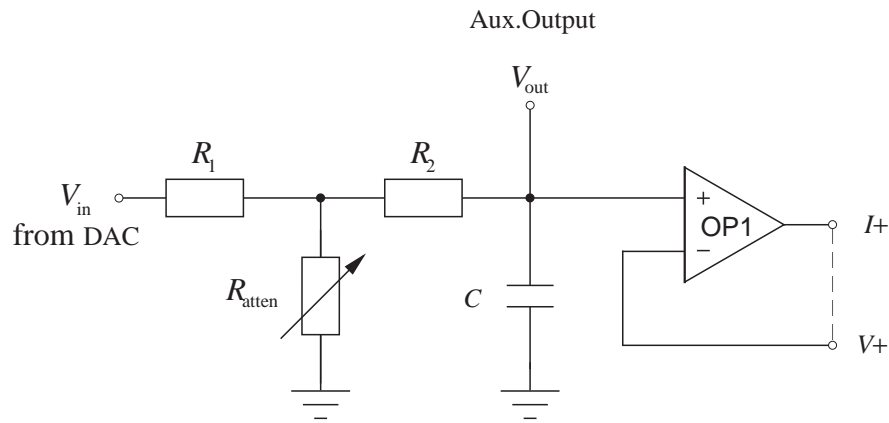


Fig. A.2. Voltage divider and RC filter at the input to the sample-biasing electronics.

where V_{in} is the voltage applied to the RC network and V_{out} is the voltage at the input to OP1. With $R_1 = R_2 = 10 \text{ k}\Omega$ and R_{atten} values from $1 \text{ }\Omega$ to $1 \text{ k}\Omega$ (in a 1–3–5 sequence), the full-scale sample bias for maximum DAC output of 10 V could be varied from 1 mV to 0.9 V . The filter was used primarily to reduce noise in the d.c. measurement of current, so the time constant was chosen to be much smaller than the time between voltage steps (45 ms , but potentially $< 1 \text{ ms}$). In addition, this attenuation was applied to the a.c. modulation, which was superimposed on the d.c. voltage before the potential divider, so the cut-off frequency was set even higher to prevent filtering of the 1 kHz modulation signal. With $C = 2 \text{ nF}$ the -3 dB frequency changes from 7.3 kHz to 8.0 kHz as R_{atten} is adjusted over its full range. A better arrangement would be to attenuate and filter the d.c. bias before adding the modulation and to set the filter cut-off frequency to remove DAC noise at the modulation frequency.

If OP1 acts as an ideal follower the voltage across the sample is identical to the voltage at the non-inverting input to OP1, with no phase shift or change in amplitude between the two. Measurement of the modulation amplitude and adjustment of the phase may then be more conveniently done using a single-ended input lock-in amplifier connected to the input of OP1. By measuring the voltage at this point and across the sample it was found that the phase shift and amplitude change were negligible for frequencies below 10 kHz and for typical sample impedances. When the circuit is operated above this limit additional phase shifts of unknown size cause the in-phase and quadrature outputs of the lock-in to be an inseparable mixture of the capacitance and conductance signals. An improvement to the circuit suggested by Holden (1992) would be to include a two-pole reed-relay switch controlled by the CIL6580 that allows the differential amplifier to be switched from across the sample to across the sensing resistor. This would allow the conductance and the capacitance of the sample to be measured separately even at high frequencies.

A.C. stability of the active voltage-biasing electronics is analysed by Speakman (1992, sec.3.5.4.1). The circuits described in this appendix have a larger phase margin, but a 15 pF capacitance was still used across the OPA111 op-amps to provide additional stabilising feedback at high frequencies (> 1 MHz). No difficulties were experienced with instability, even with dummy samples of large capacitance.

A.1.1.2 Differential Amplifier

An INA110 instrumentation amplifier was used to amplify the voltage drop across the sensing resistor and to isolate the sample-biasing electronics from the lower-quality input amplifiers of the CIL6580. The INA110 has low bias current (50 pA), very low gain drift and low offset drift so allows accurate measurements of small nanoamp currents. The manufacturer's recommended PCB layout was used and the gain was set to 200. The input leads were actively shielded by an OPA121 buffer driven by an average of the input voltages, available on pin 3*. The offset voltage was nulled using an OPA27 buffer to the reference (pin 6). This prevents degradation of offset voltage drift. The offset current, measured with no sample connected, was typically smaller than 0.1% of the full-scale current and had a standard deviation (a measure of the noise in the current) of less than 0.01%.

A.1.1.3 Noise and Shielding

Most experiments carried out in this work had sample resistances of $10\text{ k}\Omega - 10\text{ M}\Omega$ and measurements were made with the sample biased between ± 200 mV. Typical currents were less than 10 nA so effort was made to minimise noise pickup and to reduce current offsets to pA levels.

All electronic circuits were constructed on PCBs, which had lower noise levels than prototype circuits built on veroboard. All PCB signal tracks were placed next to wide ground tracks and extensive use was made of ground planes. Wide tracks were also used for the power supply lines, which were connected to ground close to each op-amp by decoupling capacitors. Connections to the PCB were made using miniature BNC cable via SMC connectors. In addition to reducing pickup, these connectors allowed the board to be removed easily from its diecast aluminium box for repair or adjustment.

An outline of the grounding and shielding of the electronics is shown in figure A.3. This shows that there are no ground loops and that the signal and signal reference voltages have been carefully shielded. Low-noise co-axial cable was used for the

* This is actually the average plus a large offset of -1.1V . Because the a.c. voltage follows the input the active shields are still effective.

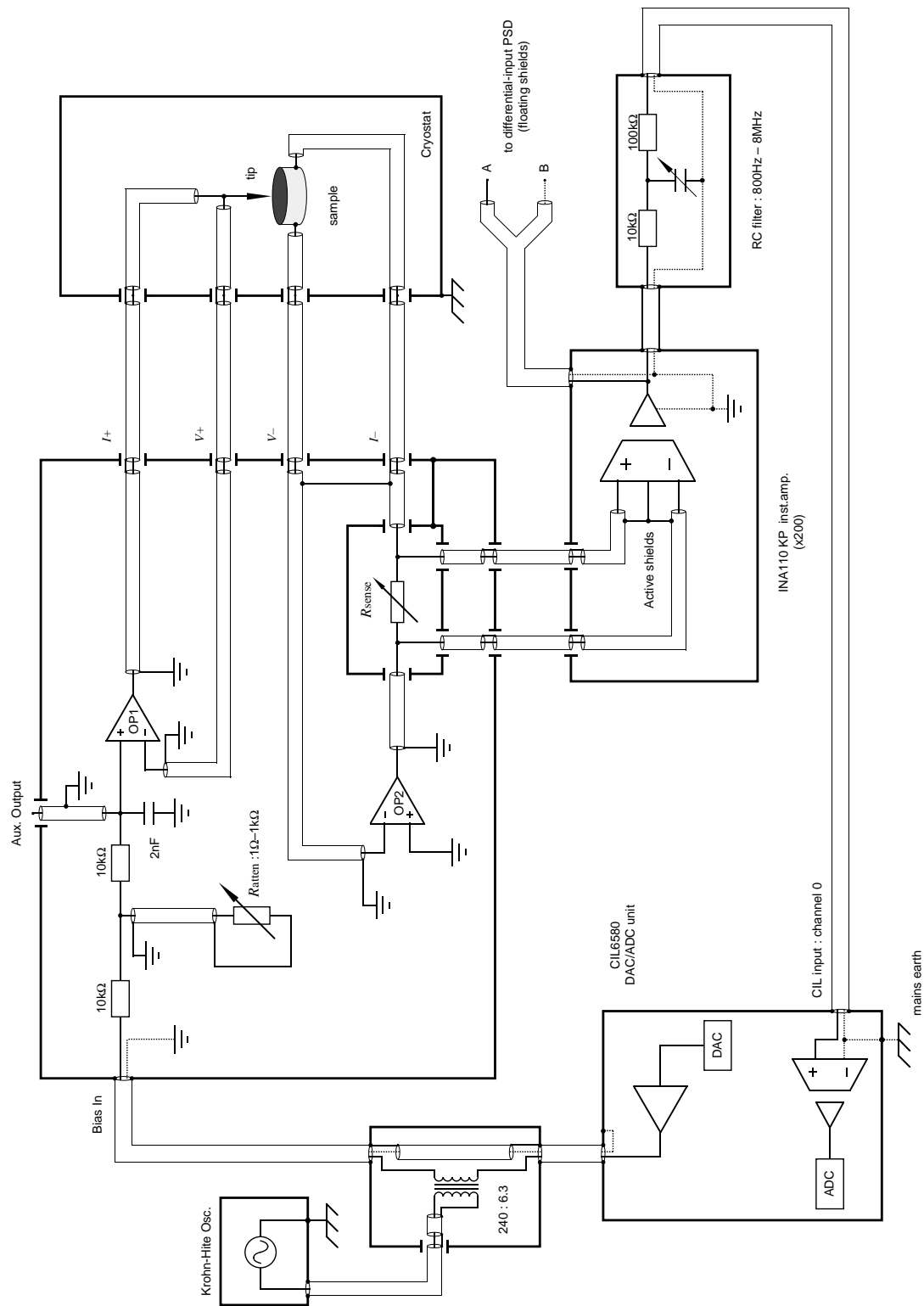


Fig. A.3. Outline of the electronics shielding and grounding.

sample leads that connected the electronics to the cryostat. Unfortunately there was not sufficient space on the cryostat's top plate for four BNC sockets so the shielding had to be broken over a short distance to admit the wires into the cryostat via a nine-pin feedthrough. Inside the cryostat the sample wires, in addition to being fed through grounded metal tubing and routed as near to the sample and tip as possible, were made from low-temperature co-axial wire*. A few millimetres of thin unshielded copper wire made the final connection between the co-ax cable and the sample. High-voltage leads to the piezotube entered the cryostat through a separate feedthrough and were fed down a separate metal tube. At all times the signal and high-voltage leads were kept far apart to minimise pickup.

Circuit ground of the sample-biasing electronics was defined at the source of the bias voltage (i.e., ground of the CIL6580's DAC) and was connected to the source by screened twisted-pair cable. Similarly, circuit ground of the instrumentation amplifier was defined by the ground of the recording electronics (i.e., ground of the CIL6580's input amplifier). The sample-biasing electronics and instrumentation amplifier were powered by separate floating-earth power supply units. The op-amps used 'star-point' grounding and power lines wherever possible and the shielding was connected to earth at only one point. The principles guiding this choice of circuit layout are described by Morrison (1986).

A.1.1.4 Calibration Errors

The calibration expressions, calculated in chapter 5, were derived by assuming that all current flowing through the sample also passed through the balance (or sense) impedance. In practice, the instrumentation amplifier, op-amps and lock-in amplifier have finite input impedances and input bias currents, which become significant with large impedance samples ($>1 \text{ M}\Omega$). The d.c. input bias current of OP3 ($< 50 \text{ pA}$) causes an offset in the measured I - V characteristic (i.e., there appears to be a small current at zero sample bias); however, this could be compensated for at run time as described in section 5.2.1. There is a smaller d.c. leakage current into the $V+$ and $V-$ sense leads due to the input bias currents of OP1 and OP2 ($< 1 \text{ pA}$). This contributes slightly to the current offset but also affects the bias across the sample due to the resulting voltage drop between the inverting input of the op-amps and the sample. Empirical measurements of current offset, noise and errors in known conductances measured with the d.c. measurement system are described in section 5.2.1.

* Lake Shore Cryotronics, Inc. Type C.

A.1.2 Modulation Broadening

This section analyses the method of measuring derivatives of a function $f(v)$ by superimposing a small sinusoidal modulation, $A \cos \omega t$, on a d.c. bias, v_0 , and time averaging the resulting signal using a lock-in amplifier. The lock-in actually measures the r.m.s. amplitude of the ω or 2ω component of a Fourier series expansion of $f(v_0 + A \cos \omega t)$. This may be represented by

$$s_m(v_0) = \frac{\sqrt{2}}{T} \int_{-T/2}^{T/2} f(v_0 + A \cos \omega t) \cos(m\omega t) dt \quad (\text{A.1})$$

where $s_1(v_0)$ and $s_2(v_0)$ are the ω and 2ω measurements respectively. To show how $s_m(v_0)$ is related to the derivatives consider a Taylor-series expansion of $f(v)$ about the d.c. bias voltage:

$$\begin{aligned} f(v) &= f(v_0 + A \cos \omega t) \\ &= f(v_0) + f'(v_0)A \cos \omega t + \frac{1}{2!} f''(v_0)(A \cos \omega t)^2 + \dots + \frac{1}{n!} f^{(n)}(v_0)(A \cos \omega t)^n + \dots \end{aligned}$$

Here, $f^{(n)}(v)$ is the exact n^{th} derivative of $f(v)$. Expanding powers of $A \cos \omega t$ and collecting terms with the same frequency gives, for $A \ll 1$

$$f(v) \approx f(v_0) + \frac{A^2}{4} f''(v_0) + \sum_{n>0} \frac{A^n \cos n\omega t}{2^{n-1} n!} (f^{(n)}(v_0) + O(A^2))$$

Substituting this expression into (A.1), using the orthogonality of cosines and rearranging gives

$$f^{(m)}(v_0) \approx F^{(m)}(v_0) = \frac{m!}{\sqrt{2}} \left(\frac{2}{A} \right)^m s_m(v_0) \quad m > 0 \quad (\text{A.2})$$

$F^{(m)}(v_0)$ is the approximate derivative calculated from the lock-in amplifier's output. For small A ,

$$\lim_{A \rightarrow 0} F^{(m)}(v_0) = f^{(m)}(v_0) \quad (\text{A.3})$$

But how are $f^{(m)}(v_0)$ and $F^{(m)}(v_0)$ related for finite A ? Clearly the modulation should cause the time-average function, $s_m(v_0)$, to depend on the behaviour of $f(v)$ not just at $v = v_0$ but for values of v roughly in the range $v_0 - A$ to $v_0 + A$. $F^{(m)}(v_0)$ may be represented by a convolution of the exact derivative function with a broadening function, $b_m(v)$.

$$F^{(m)}(v) = f^{(m)}(v) * b_m(v) \quad (\text{A.4})$$

To calculate $b_m(v)$ consider a test function

$$f(v) = \begin{cases} \frac{v^{m-1}}{(m-1)!} & v \geq 0 \\ 0 & v < 0 \end{cases}$$

For this particular function, substituting (A.1) into (A.2) gives

$$F^{(m)}(v) = \frac{2^m m}{\pi A} \int_0^{\cos^{-1}(-v/A)} \left(\frac{v}{A} + \cos \theta \right)^{m-1} \cos(m\theta) d\theta \quad (\text{A.5})$$

The m^{th} derivative of the test function is the delta function so (A.4) simplifies to

$$\begin{aligned} F^{(m)}(v) &= f^{(m)}(v) * b_m(v) \\ &= \delta(v) * b_m(v) \\ &= b_m(v) \end{aligned}$$

and (A.5) is exactly the broadening function, $b_m(v)$. This may easily be evaluated to give

$$b_1(v) = \frac{2}{\pi A^2} \text{Re} \left(\sqrt{A^2 - v^2} \right) \quad (\text{A.6})$$

and

$$b_2(v) = \frac{8}{3\pi A^4} \text{Re} \left(\sqrt{A^2 - v^2} \right)^3 \quad (\text{A.7})$$

Although these were calculated for a special case, the broadening function should be independent of $f(v)$ and (A.6) and (A.7) are true in general. The FWHM of $b_1(v)$ and $b_2(v)$ are $A\sqrt{3}$ and $1.22A$ respectively. A is usually chosen so that modulation broadening is equal to thermal broadening, which has width $5.4 k_B T$ for inelastic tunnelling (3.22) and $3.5 k_B T$ for elastic tunnelling (3.15–17).

Modulation-like additional broadening, observed by Speakman (1992, sec.3.7.4.3) in high-resistance samples ($>10 \text{ k}\Omega$) and attributed to high-frequency noise from the voltage source, was not noted as a problem.

A.2 Servo Control of the Tunnelling Tip

The tip was advanced towards the sample by a motor-driven differential screw, controlled by the circuit shown in figure A.4. During this advance the piezotube was extended by applying -100 V to the inner electrode. The motor and piezotube voltages were applied via reed relays which were energised if the input to the relay

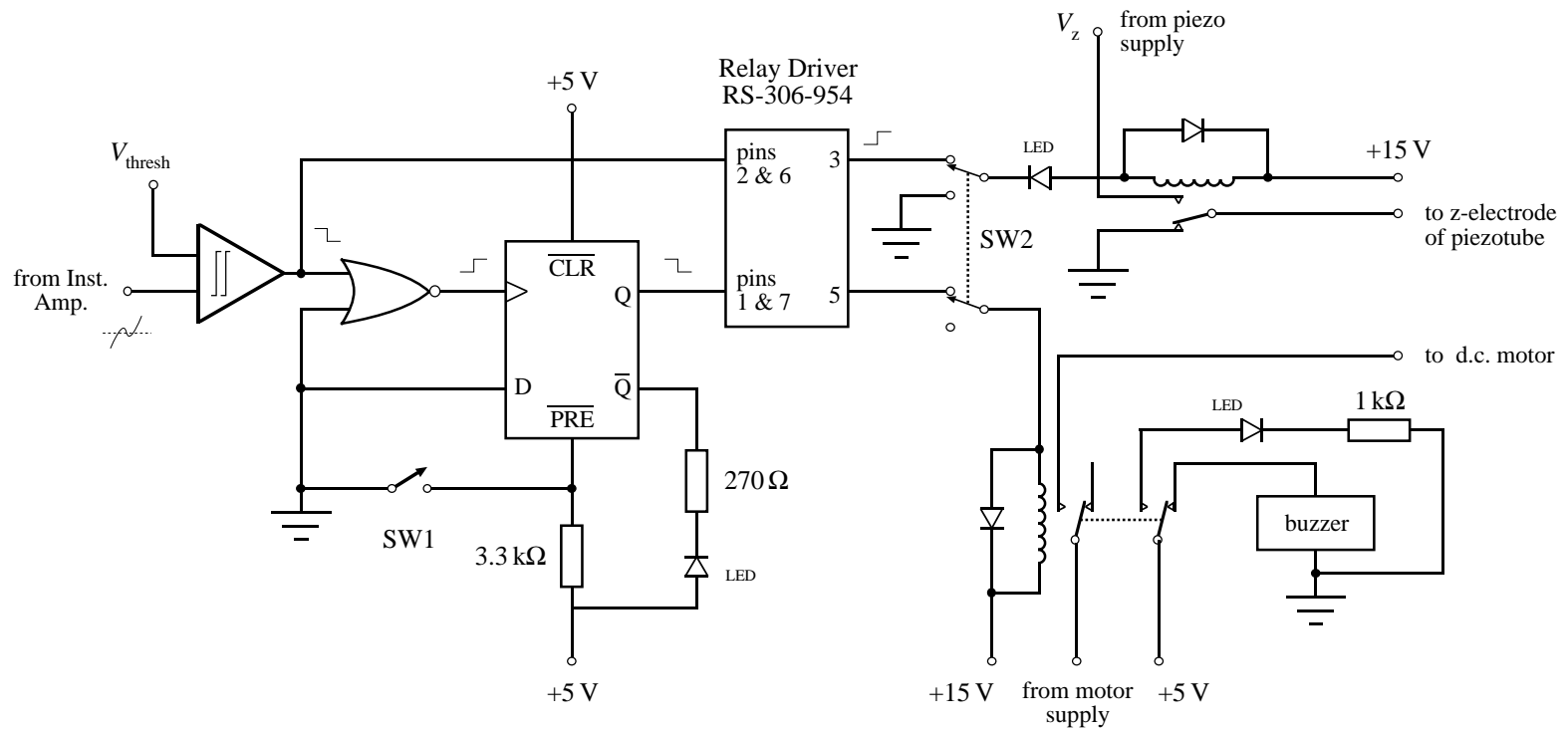


Fig. A.4. Threshold detector and latch circuit used to control the coarse stage of tip-sample approach.

driver was high. This state was pre-set by briefly closing switch SW1. Initially the tip was far from the sample's surface so no tunnel current flowed and the output of the instrumentation amplifier in the current-voltage measuring electronics was well below the Schmitt trigger's comparison voltage, V_{thresh} . The output of the Schmitt trigger was then high and the NOR gate gave a low at the clock input of the D-type flip-flop. When the tip made contact with the sample the current rose above the threshold voltage and the Schmitt trigger output dropped. The NOR gate gave a rising edge at the clock input so the low at the D-input was passed to the output and the relay driver turned off. Both the piezotube and motor voltages were cut, retracting the tip and stopping the motor. The system stayed latched in this state until SW1 was closed again. By closing switch SW2 the servomechanism was bypassed (i.e., the piezotube was permanently energised and motor was off) so the piezotube could be manually controlled.

The Schmitt trigger was built with a 311 comparator (Horowitz and Hill 1980, fig.3.54) and had a fixed threshold voltage of 4 V. The corresponding threshold current could be changed by adjusting R_{sense} . Audio and visual indicators were incorporated into the circuit to warn of triggering events and to show clearly which relays were turned on.

Figure A.4 illustrates the servocontrol circuit just after a triggering event. The piezotube is retracted, the motor and LEDs are off and the buzzer is on.